

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-20 (canceled)

1 **Claim 21 (new):** A semiconductor device design method
2 for forming a semiconductor device by combining and placing
3 previously registered functional blocks, and determining a
4 wiring pattern in accordance with given logical circuit
5 specifications, and design method comprising:

6 a registration step of previously registering a first
7 functional block having a first conduction type diode
8 comprising a first conduction type diffusion layer
9 connected to an input pin of the functional block, and a
10 second conduction type well connected to a second power
11 supply or a second conduction type diode comprising a
12 second conduction type diffusion layer connected to the
13 input pin and a first conduction type well connected to a
14 first power supply and a second functional block having the
15 same logic as and the same drive capability as the first
16 functional block but not containing the first or second
17 conduction type diode;

18 a determination step of determining whether or not a
19 wiring conductor conducting to the input pin and a gate

20 electrode becomes an antenna ratio exceeding an allowed
21 antenna ratio in said semiconductor device; and
22 a selection step of selectively using the first
23 functional block, if said determination step determines
24 that the input pin conducts to the gate electrode exceeding
25 the antenna ratio.

1 **Claim 22 (new):** A semiconductor device formed by
2 combining and placing previously registered functional
3 blocks, and determining a wiring pattern in accordance with
4 given logical circuit specifications, said semiconductor
5 device comprising:

6 a first functional block including at least one of:
7 a first conduction type diode having a first
8 conduction type diffusion layer connected to an input pin
9 of the first functional block and a second conduction type
10 well connected to a second power supply, and

11 a second conduction type diode having a second
12 conduction type diffusion layer connected to the input pin
13 and a first conduction type well connected to a first power
14 supply; and

15 a second functional block including the same logic as
16 the first functional block but not containing said first or
17 second conduction type diode,

18 wherein either the first functional block or the
19 second functional block is selectively used depending on

20 whether or not a wiring conductor conducting to the input
21 pin and a gate electrode becomes an antenna ratio exceeding
22 an allowed antenna ratio in said semiconductor device.

1 **Claim 23 (new):** A semiconductor device design method
2 for forming a semiconductor device by combining and placing
3 previously registered functional blocks, and determining a
4 wiring pattern in accordance with given logical circuit
5 specifications, and design method comprising:

6 a registration step of previously registering a first
7 functional block having a first conduction type diode
8 comprising a first conduction type diffusion layer
9 connected to an input pin of the functional block, and a
10 second conduction type well connected to a second power
11 supply or a second conduction type diode comprising a
12 second conduction type diffusion layer connected to the
13 input pin and a first conduction type well connected to a
14 first power supply and a second functional block having the
15 same logic as the first functional block but not containing
16 the first or second conduction type diode;

17 a determination step of determining whether or not a
18 wiring conductor conducting to the input pin and a gate
19 electrode becomes an antenna ratio exceeding an allowed
20 antenna ratio in said semiconductor device; and

21 a selection step of selectively using the first
22 functional block, if said determination step determines

23 that the input pin conducts to the gate electrode exceeding
24 the antenna ratio.

1 **Claim 24 (new):** A computer-readable recording medium
2 storing the semiconductor device design method as claimed
3 in claim 23 as a program for causing a computer to execute
4 the semiconductor device design method.

1 **Claim 25 (new):** A semiconductor device design support
2 system for automatically forming a semiconductor device by
3 combining and placing previously registered functional
4 blocks, and determining a wiring pattern in accordance with
5 given logical circuit specifications, said design support
6 system comprising:

7 registration means for previously registering a first
8 functional block having a first conduction type diode
9 comprising a first conduction type diffusion layer
10 connected to an input pin of the functional block, and a
11 second conduction type well connected to a second power
12 supply or a second conduction type diode comprising a
13 second conduction type diffusion layer connected to the
14 input pin and a first conduction type well connected to a
15 first power supply and a second functional block having the
16 same logic as the first functional block but not containing
17 the first or second conduction type diode;

18 determination means for determining whether or not a
19 wiring conductor conducting to the input pin and a gate
20 electrode becomes an antenna ratio exceeding an allowed
21 antenna ratio in said semiconductor device; and

22 selection means for selectively using the first
23 functional block, if said determination step determines
24 that the input pin conducts to the gate electrode exceeding
25 the antenna ratio.